



CMOS ASYNCHRONOUS FIFO

256 x 9, 512 x 9 and 1,024 x 9

IDT7200L
IDT7201LA
IDT7202LA

FEATURES:

- First-In/First-Out dual-port memory
- 256 x 9 organization (IDT7200)
- 512 x 9 organization (IDT7201)
- 1,024 x 9 organization (IDT7202)
- Low power consumption
 - Active: 440mW (max.)
 - Power-down: 28mW (max.)
- Ultra high speed—12ns access time
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Pin and functionally compatible with 720X family
- Status Flags: Empty, Half-Full, Full
- Auto-retransmit capability
- High-performance CEMOS™ technology
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-87531, 5962-89666, 5962-89863 and 5962-89536 are listed on this function
- Dual versions available in the TSSOP package. For more information, see IDT7280/7281/7282 data sheet
 - IDT7280 = 2 x IDT7200
 - IDT7281 = 2 x IDT7201
 - IDT7282 = 2 x IDT7202

- Industrial temperature range (-40°C to +85°C) is available (plastic packages only)
- Green parts available, see ordering information

DESCRIPTION:

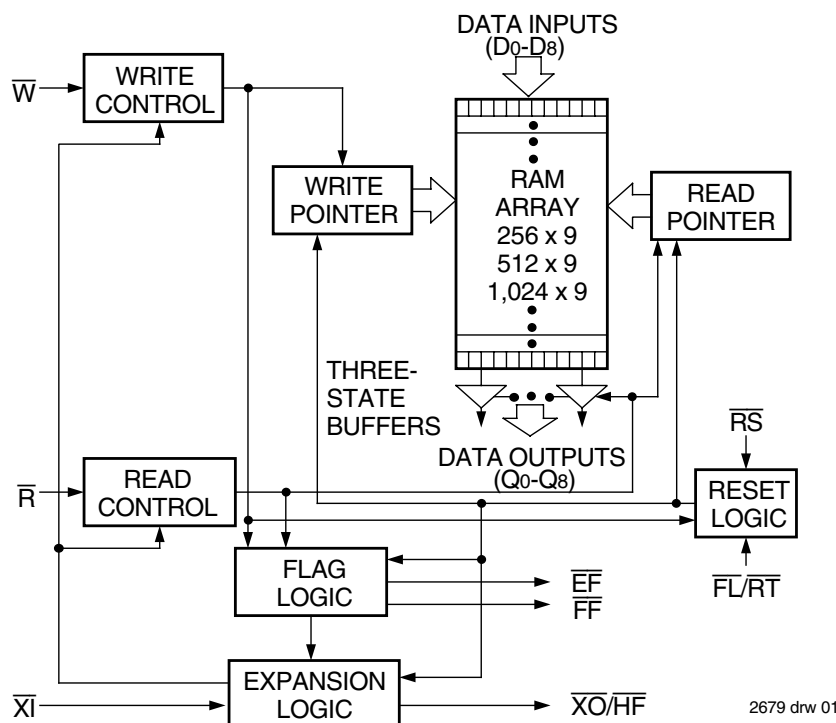
The IDT7200/7201/7202 are dual-port memories that load and empty data on a first-in/first-out basis. The devices use Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the devices through the use of the Write (\bar{W}) and Read (\bar{R}) pins.

The devices utilize a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also features a Retransmit (\bar{RT}) capability that allows for reset of the read pointer to its initial position when \bar{RT} is pulsed LOW to allow for retransmission from the beginning of data. A Half-Full Flag is available in the single device mode and width expansion modes.

These FIFOs are fabricated using IDT's high-speed CMOS technology. They are designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

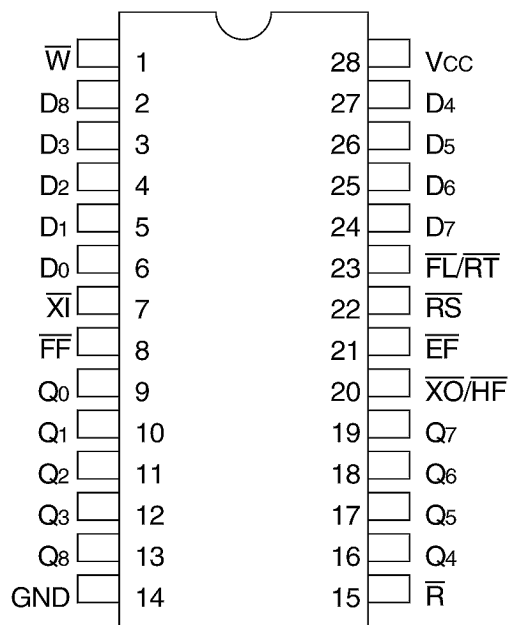
FUNCTIONAL BLOCK DIAGRAM



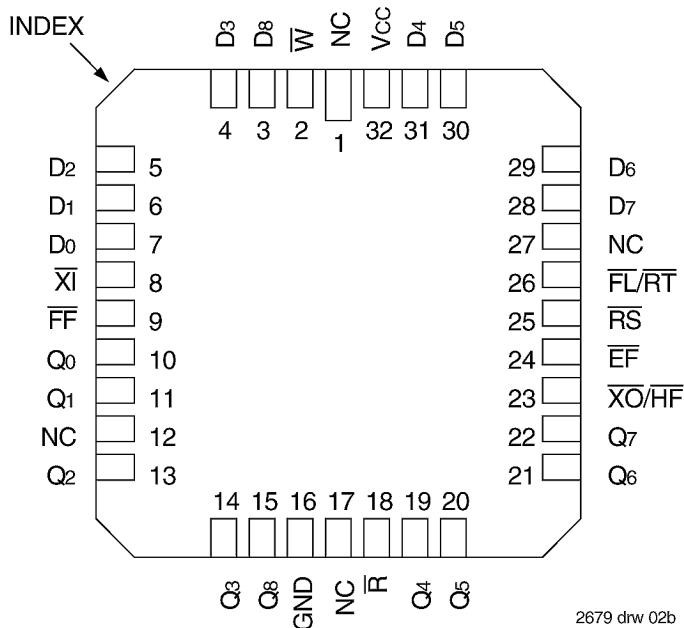
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COMMERCIAL, INDUSTRIAL AND MILITARY TEMPERATURE RANGES

PIN CONFIGURATIONS



2679 drw 02a



2679 drw 02b

Package Type	Reference Identifier	Order Code
PLASTIC DIP ⁽¹⁾	P28-1	P
PLASTIC THIN DIP	P28-2	TP
CERDIP ⁽¹⁾	D28-1	D
THIN CERDIP	D28-3	TD
SOIC	S028-3	SO

TOP VIEW

Package Type	Reference Identifier	Order Code
LCC ⁽¹⁾	L32-1	L
PLCC	J32-1	J

TOP VIEW

NOTE:

1. The 600-mil-wide DIP (P28-1 and D28-1) and LCC are not available for the IDT7200.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Com'l & Ind'l	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TSTG	Storage Temperature	-55 to +125	-65 to +155	°C
IOUT	DC Output Current	-50 to +50	-50 to +50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage Commercial/Industrial/Military	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V _{IH} ⁽¹⁾	Input High Voltage Com'l/Ind'l	2.0	—	—	V
V _{IH} ⁽¹⁾	Input High Voltage Military	2.2	—	—	V
V _{IL} ⁽²⁾	Input Low Voltage Commercial/Industrial/Military	—	—	0.8	V
TA	Operating Temperature Commercial	0	—	70	°C
TA	Operating Temperature Industrial	-40	—	85	°C
TA	Operating Temperature Military	-55	—	125	°C

NOTES:

- For $\overline{RT}/RS/XI$ input, V_{IH} = 2.6V (commercial).
For $\overline{RT}/RS/XI$ input, V_{IH} = 2.8V (military).
- 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: $V_{CC} = 5V \pm 10\%$, $T_A = 0^\circ C$ to $+70^\circ C$; Industrial: $V_{CC} = 5V \pm 10\%$, $T_A = -40^\circ C$ to $+85^\circ C$; Military: $V_{CC} = 5V \pm 10\%$, $T_A = -55^\circ C$ to $+125^\circ C$)

Symbol	Parameter	IDT7200L IDT7201LA IDT7202LA Com'l & Ind'l ⁽¹⁾ $t_A = 12, 15, 20, 25, 35, 50$ ns		IDT7200L IDT7201LA IDT7202LA Military ⁽²⁾ $t_A = 20, 30, 50, 80$ ns		Unit
		Min.	Max.	Min.	Max.	
$I_{LI}^{(3)}$	Input Leakage Current (Any Input)	-1	1	-10	10	μA
$I_{LO}^{(4)}$	Output Leakage Current	-10	10	-10	10	μA
V_{OH}	Output Logic "1" Voltage $I_{OH} = -2mA$	2.4	—	2.4	—	V
V_{OL}	Output Logic "0" Voltage $I_{OL} = 8mA$	—	0.4	—	0.4	V
$I_{CC1}^{(5,6,7)}$	Active Power Supply Current	—	80	—	100	mA
$I_{CC2}^{(5,8)}$	Standby Current ($\overline{R}=\overline{W}=\overline{RS}=\overline{FL}/\overline{RT}=V_{IH}$)	—	5	—	15	mA

NOTES:

- Industrial temperature range product for the 15ns and 25 ns speed grades are available as a standard device.
- Military speed grades of 50ns and 80ns are only available for the IDT7201LA.
- Measurements with $0.4 \leq V_{IN} \leq V_{CC}$.
- $\overline{R} \geq V_{IH}$, $0.4 \leq V_{OUT} \leq V_{CC}$.
- Tested with outputs open ($I_{OUT} = 0$).
- Tested at $f = 20$ MHz.
- Typical $I_{CC1} = 15 + 2*fs + 0.02*Cl*fs$ (in mA) with $V_{CC} = 5V$, $T_A = 25^\circ C$, $fs = WCLK$ frequency = RCLK frequency (in MHz, using TTL levels), data switching at $fs/2$, $Cl =$ capacitive load (in pF).
- All Inputs = $V_{CC} - 0.2V$ or $GND + 0.2V$.

CAPACITANCE ($T_A = +25^\circ C$, $f = 1.0$ MHz)

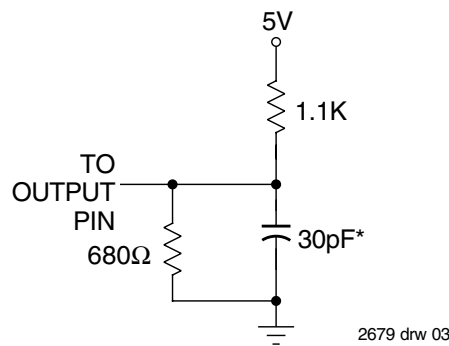
Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	8	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	pF

NOTE:

- Characterized values, not currently tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1



or equivalent circuit

Figure 1. Output Load

* Includes scope and jig capacitances.

AC ELECTRICAL CHARACTERISTICS⁽¹⁾

(Commercial: VCC = 5V ± 10%, TA = 0°C to +70°C; Industrial: VCC = 5V ± 10%, TA = -40°C to +85°C; Military: VCC = 5V ± 10%, TA = -55°C to +125°C)

Symbol	Parameter	Commercial		Com'l & Ind'l ⁽²⁾		Com'l & Mil.		Com'l & Ind'l ⁽²⁾		Unit
		IDT7200L12 IDT7201LA12 IDT7202LA12		IDT7200L15 IDT7201LA15 IDT7202LA15		IDT7200L20 IDT7201LA20 IDT7202LA20		IDT7200L25 IDT7201LA25 IDT7202LA25		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tS	Shift Frequency	—	50	—	40	—	33.3	—	28.5	MHz
tRC	Read Cycle Time	20	—	25	—	30	—	35	—	ns
tA	Access Time	—	12	—	15	—	20	—	25	ns
tRR	Read Recovery Time	8	—	10	—	10	—	10	—	ns
tRPW	Read Pulse Width ⁽³⁾	12	—	15	—	20	—	25	—	ns
tRLZ	Read Pulse Low to Data Bus at Low Z ⁽⁴⁾	3	—	3	—	3	—	3	—	ns
tWLZ	Write Pulse High to Data Bus at Low Z ^(4,5)	5	—	5	—	5	—	5	—	ns
tDV	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	ns
tRHZ	Read Pulse High to Data Bus at High Z ⁽⁴⁾	—	12	—	15	—	15	—	18	ns
tWC	Write Cycle Time	20	—	25	—	30	—	35	—	ns
tWPW	Write Pulse Width ⁽³⁾	12	—	15	—	20	—	25	—	ns
tWR	Write Recovery Time	8	—	10	—	10	—	10	—	ns
tDS	Data Set-up Time	9	—	11	—	12	—	15	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tRSC	Reset Cycle Time	20	—	25	—	30	—	35	—	ns
tRS	Reset Pulse Width ⁽³⁾	12	—	15	—	20	—	25	—	ns
tRSS	Reset Set-up Time ⁽⁴⁾	12	—	15	—	20	—	25	—	ns
tRSR	Reset Recovery Time	8	—	10	—	10	—	10	—	ns
tRTC	Retransmit Cycle Time	20	—	25	—	30	—	35	—	ns
tRT	Retransmit Pulse Width ⁽³⁾	12	—	15	—	20	—	25	—	ns
tRTS	Retransmit Set-up Time ⁽⁴⁾	12	—	15	—	20	—	25	—	ns
tRTR	Retransmit Recovery Time	8	—	10	—	10	—	10	—	ns
tEFL	Reset to Empty Flag Low	—	12	—	25	—	30	—	35	ns
tHFH,FFH	Reset to Half-Full and Full Flag High	—	17	—	25	—	30	—	35	ns
tRTF	Retransmit Low to Flags Valid	—	20	—	25	—	30	—	35	ns
tREF	Read Low to Empty Flag Low	—	12	—	15	—	20	—	25	ns
tRFF	Read High to Full Flag High	—	14	—	15	—	20	—	25	ns
tRPE	Read Pulse Width after EF High	12	—	15	—	20	—	25	—	ns
tWEF	Write High to Empty Flag High	—	12	—	15	—	20	—	25	ns
tWFF	Write Low to Full Flag Low	—	14	—	15	—	20	—	25	ns
tWHF	Write Low to Half-Full Flag Low	—	17	—	25	—	30	—	35	ns
tRHF	Read High to Half-Full Flag High	—	17	—	25	—	30	—	35	ns
tWPF	Write Pulse Width after FF High	12	—	15	—	20	—	25	—	ns
tXOL	Read/Write to X̄O Low	—	12	—	15	—	20	—	25	ns
tXOH	Read/Write to X̄O High	—	12	—	15	—	20	—	25	ns
tXI	X̄I Pulse Width ⁽³⁾	12	—	15	—	20	—	25	—	ns
tXIR	X̄I Recovery Time	8	—	10	—	10	—	10	—	ns
tXIS	X̄I Set-up Time	8	—	10	—	10	—	10	—	ns

NOTES:

1. Timings referenced as in AC Test Conditions.
2. Industrial temperature range product for 15ns and 25ns speed grades are available as a standard device.
3. Pulse widths less than minimum value are not allowed.
4. Values guaranteed by design, not currently tested.
5. Only applies to read data flow-through mode

AC ELECTRICAL CHARACTERISTICS⁽¹⁾ (Continued)

(Commercial: VCC = 5V ± 10%, TA = 0°C to +70°C; Industrial: VCC = 5V ± 10%, TA = -40°C to +85°C; Military: VCC = 5V ± 10%, TA = -55°C to +125°C)

Symbol	Parameter	Military		Commercial		Com'l & Mil. ⁽²⁾		Military ⁽²⁾		Unit
		IDT7200L30 IDT7201LA30 IDT7202LA30		IDT7200L35 IDT7201LA35 IDT7202LA35		IDT7200L50 IDT7201LA50 IDT7202LA50		IDT7201LA80		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tS	Shift Frequency	—	25	—	22.2	—	15	—	10	MHz
tRC	Read Cycle Time	40	—	45	—	65	—	100	—	ns
tA	Access Time	—	30	—	35	—	50	—	80	ns
tRR	Read Recovery Time	10	—	10	—	15	—	20	—	ns
tRPW	Read Pulse Width ⁽³⁾	30	—	35	—	50	—	80	—	ns
tRLZ	Read Pulse Low to Data Bus at Low Z ⁽⁴⁾	3	—	3	—	3	—	3	—	ns
tWLZ	Write Pulse High to Data Bus at Low Z ^(4,5)	5	—	5	—	5	—	5	—	ns
tDV	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	ns
tRHZ	Read Pulse High to Data Bus at High Z ⁽⁴⁾	—	20	—	20	—	30	—	30	ns
tWC	Write Cycle Time	40	—	45	—	65	—	100	—	ns
tWPW	Write Pulse Width ⁽³⁾	30	—	35	—	50	—	80	—	ns
tWR	Write Recovery Time	10	—	10	—	15	—	20	—	ns
tDS	Data Set-up Time	18	—	18	—	30	—	40	—	ns
tDH	Data Hold Time	0	—	0	—	5	—	10	—	ns
tRSC	Reset Cycle Time	40	—	45	—	65	—	100	—	ns
tRS	Reset Pulse Width ⁽³⁾	30	—	35	—	50	—	80	—	ns
tRSS	Reset Set-up Time ⁽⁴⁾	30	—	35	—	50	—	80	—	ns
tRSR	Reset Recovery Time	10	—	10	—	15	—	20	—	ns
tRTC	Retransmit Cycle Time	40	—	45	—	65	—	100	—	ns
tRT	Retransmit Pulse Width ⁽³⁾	30	—	35	—	50	—	80	—	ns
tRTS	Retransmit Set-up Time ⁽⁴⁾	30	—	35	—	50	—	80	—	ns
tRTR	Retransmit Recovery Time	10	—	10	—	15	—	20	—	ns
tEFL	Reset to Empty Flag Low	—	40	—	45	—	65	—	100	ns
tHFH,FFH	Reset to Half-Full and Full Flag High	—	40	—	45	—	65	—	100	ns
tRTF	Retransmit Low to Flags Valid	—	40	—	45	—	65	—	100	ns
tREF	Read Low to Empty Flag Low	—	30	—	30	—	45	—	60	ns
tRFF	Read High to Full Flag High	—	30	—	30	—	45	—	60	ns
tRPE	Read Pulse Width after \overline{EF} High	30	—	35	—	50	—	80	—	ns
tWEF	Write High to Empty Flag High	—	30	—	30	—	45	—	60	ns
tWFF	Write Low to Full Flag Low	—	30	—	30	—	45	—	60	ns
tWHF	Write Low to Half-Full Flag Low	—	40	—	45	—	65	—	100	ns
tRHF	Read High to Half-Full Flag High	—	40	—	45	—	65	—	100	ns
tWPF	Write Pulse Width after \overline{FF} High	30	—	35	—	50	—	80	—	ns
tXOL	Read/Write to \overline{XO} Low	—	30	—	35	—	50	—	80	ns
tXOH	Read/Write to \overline{XO} High	—	30	—	35	—	50	—	80	ns
tXI	\overline{XI} Pulse Width ⁽³⁾	30	—	35	—	50	—	80	—	ns
tXIR	\overline{XI} Recovery Time	10	—	10	—	10	—	10	—	ns
tXIS	\overline{XI} Set-up Time	10	—	10	—	15	—	15	—	ns

NOTES:

1. Timings referenced as in AC Test Conditions
2. Military speed grades of 50ns and 80ns are only available for IDT7201LA.
3. Pulse widths less than minimum value are not allowed.
4. Values guaranteed by design, not currently tested.
5. Only applies to read data flow-through mode.

ORDERING INFORMATION

XXXX	X	XXX	X	X	X			
Device Type	Power	Speed	Package	Process/ Temperature Range				
						Blank I ⁽¹⁾	Commercial (0°C to +70°C) Industrial (-40°C to +85°C) Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B	
						B		
						G ⁽³⁾	Green	
						P ⁽⁴⁾	Plastic DIP	P28-1 (7201 & 7202 Only)
						TP	Plastic Thin DIP	P28-2
						D	CERDIP	D28-1 (7201 & 7202 Only)
						TD	Thin CERDIP	D28-3
						J	Plastic Leaded Chip Carrier	PLCC J32-1
						SO	SOIC	SO28-3
						L	Leadless Chip Carrier	LCC L32-1 (7201 & 7202 Only)
						12	Commercial Only	} Access Time (t _A) Speed in Nanoseconds
						15	Commercial and Industrial	
						20	Commercial and Military	
						25	Commercial and Industrial	
						30	Military Only	
						35	Commercial Only	
						50	Commercial and (Military only for 7201)	
						80	Military only for 7201	
						LA ⁽²⁾	Low Power	
						7200	256 x 9-Bit FIFO	} See 7280/7281/7282 data sheet for details
						7201	512 x 9-Bit FIFO	
						7202	1,024 x 9-Bit FIFO	
						7280	256 x 9-Bit DUAL FIFO	
						7281	512 x 9-Bit DUAL FIFO	
						7282	1,024 x 9-Bit DUAL FIFO	

NOTES:

1. Industrial temperature range product is available for the 15ns and 25ns as a standard product.
2. "A" to be included for IDT7201 and IDT7202 ordering part number.
3. Green parts are available. For specific speeds and packages contact your local sales office.
4. For "P", Plastic Dip, when ordering green package, the suffix is "PDG".

2679 drw 21